first transfer gate transistor and the second pull-down transistor having a first source/drain connected to a second source/drain of said second transfer gate transistor, both first and second pull-down transistors having a second source/drain connected to a power supply voltage node; and

wherein the first and second transfer gate transistors each have a first width and include a gate oxide layer having a first thickness, the first and second pull-down transistors each have a second width and include a gate oxide layer having a second thickness, and a product of the [first] second width and the first thickness is greater than or equal to a product of the [second] first width and the second thickness.

4. The SRAM memory cell of claim 1, wherein the first and second thicknesses are determined as follows:

$$[RATIO \le \frac{Tox_{ig}}{Tox_{pd}} \quad \frac{W_{pd} / L_{pd}}{W_{ig} / L_{ig}} \quad \frac{Vcc - Vt_{ig}}{Vcc - Vt_{pd}}]$$

$$RATIO \le \frac{Tox_{lg}}{Tox_{pd}} \times \frac{W_{pd} / L_{pd}}{W_{lg} / L_{lg}} \times \frac{Vcc - Vt_{pd}}{Vcc - Vt_{lg}}$$

where RATIO is the desired ratio of the transfer gate transistors and the pull down transistors, Tox_{tg} is the gate oxide thickness of the transfer gate transistor, Tox_{pd} is the gate oxide thickness of the pull-down transistor, W_{pd} is width of the pull-down transistor, L_{pd} is the length of the pull-down transistor, W_{tg} is the width of the transfer gate transistor, L_{tg} is the length of the transfer gate transistor, V_{tg} is the threshold voltage of the transfer gate transistor, and V_{tpd} is the threshold voltage of the pull-down transistor.

- 6. A semiconductor circuit comprising:
- a first transistor having a first width an a first gate including a gate oxide layer having a first thickness; and
- a second transistor having a second width and a second gate including a gate oxide layer having a second thickness, wherein a product of the [second]

as

<u>first</u> width and the second thickness is greater than a product of the [first] <u>second</u> width and the first thickness.

9. The semiconductor circuit of claim 8, wherein the gate oxide thickness of the pull-down transistor and a transfer gate transistor in the SRAM memory cell are selected using the following:

$$\begin{split} & [\text{RATIO} \leq \frac{Tox_{lg}}{Tox_{pd}} \ \frac{W_{pd} / L_{pd}}{W_{lg} / L_{lg}} \ \frac{Vcc - Vt_{lg}}{Vcc - Vt_{pd}}] \\ & \text{RATIO} \leq \frac{Tox_{lg}}{Tox_{pd}} \ x \ \frac{W_{pd} / L_{pd}}{W_{lg} / L_{lg}} \ x \ \frac{Vcc - Vt_{pd}}{Vcc - Vt_{lg}} \end{split}$$

where RATIO is the desired ratio of the transfer gate transistors and the pull down transistors and the pull-down transistors, Tox_{tg} is the gate oxide thickness of the transfer gate transistor, Tox_{pd} is the gate oxide thickness of the pull-down transistor, W_{pd} is width of the pull-down transistor, L_{pd} is the length of the pull-down transistor, W_{tg} is the width of the transfer gate transistor, L_{tg} is the length of the transfer gate transistor, V_{tg} is the threshold voltage of the transfer gate transistor, and V_{tpd} is the threshold voltage of the pull-down transistor.

Please add the following new claims:

- 13. A semiconductor circuit, comprising:
- a first transistor including a first gate having a first width and including a first gate insulator having a first thickness; and
- a second transistor including a second gate having a second width and including a second gate insulator having a second thickness, a product of the first width and the second thickness being greater than or equal to a product of the second width and the first thickness.

- 14. The semiconductor circuit of claim 13 wherein the first transistor comprises a pull-down transistor.
- 15. The semiconductor circuit of claim 13 wherein the second transistor comprises a transfer gate transistor.
- 16. The semiconductor circuit of claim 13 wherein the product of the first width and the second thickness is greater than the product of the second width and the first thickness.
- 17. A semiconductor circuit, comprising:
- a first transistor including a first channel region having a first width and including a first gate insulator having a first thickness; and
- a second transistor including a second channel region having a second width and including a second gate insulator having a second thickness, a product of the first width and the second thickness being greater than or equal to a product of the second width and the first thickness.
- 18. The semiconductor circuit of claim 17 wherein the first transistor comprises a pull-down transistor.
- 19. The semiconductor circuit of claim 17 wherein the second transistor comprises a transfer gate transistor.
 - 20. The semiconductor circuit of claim 17 wherein the product of the first width and the second thickness is greater than the product of the second width and the first thickness.
 - 21. A memory cell. comprising:
 - a pull-down transistor including a first gate having a first width and including a first gate insulator having a first thickness; and